

Introduction to the Artemis CCD Camera

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Introduction to the Artemis CCD Camera..	1
Introduction.....	3
A brief introduction to astronomical CCD cameras.....	4
The Artemis CCD camera.....	6
The CCD.....	6
Signal conditioning pre ADC.....	6
Analogue to digital conversion.....	7
The Processor.....	7
Peripherals.....	7
Expansion port.....	7
USB chipset.....	8
FIFO memory.....	8
Credits.....	9
QCUIAG.....	9
Mechanical Design.....	9
PCB Layout.....	9
Beta testers.....	9

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Introduction

The camera project grew out of a slightly simpler idea Jon Grove and myself had to add a 12+ bit analogue to digital converter (ADC) to a modified security camera and use a small microcontroller and USB link to interface with a PC. From memory it took several months to choose suitable components and get to the stage of a working prototype. This used the microcontroller to control the exposure and the ADC digitised the video signal a pixel at a time. A early picture was posted to QCUIAG to announce the project and I believed development work was nearly finished. Then Jon suggest that as we had a working 'back end' we could go the whole hog and make a CCD camera from scratch. It didn't sound like much work at the time!

Although some parts of the camera development might appear hap hazard we have been an surprisingly consistence when applying a number of goals for the project. Perhaps the most important is the desire to share our interest in CCD cameras and electronics. The first book I read on CCD imaging was the CCD camera cookbook. This gave complete instruction on making a cooled astronomical CCD camera. The design is a little dated now but the principle of being able to build and learn at the same time is still very powerful. Although I never made a cookbook camera I have read the book itself many times and learnt much.

Throughout the project we have aimed to use current, tried and tested hardware rather than the latest bleeding edge approaches. This playing it safe has probably prevented us getting bogged down in 'novel' problems and also allowed us to use more cost effective components. These choices are particularly evident in the choice of readout speed of the camera's CCD. Its fast compared with the old parallel port cameras but relatively slow when compared to USB2 offerings from SX and SBIG. However by not chasing readout speed as a main goal it has allowed us more leeway with the components optimised to image quality.

Where possible we have tried to be innovative. This is not particularly easy for non-professionals in electronics, a field where datasheets and reference designs abound. As our experience is with software rather than the hardware we have where possible moved the cameras functionality into the digital domain. Its here where we can start to innovate a bit. So the hardware side of the camera has ended up about as simple and minimal as we could make it. In so doing we have ended up with a remarkably flexible platform on which to build these cameras. Functions such as the multi CCD compatibility, multi readout modes, expansion potential stem from having a simple hardware design.

The camera is never finished. With many electronics projects once the last solder joint has cooled that's about it. For this camera we would like to see the completion of the basic kit as just the start! The camera has a dedicated expansion port and the firmware is included to communicate with other devices over this link. There are many possible enhancements both software and hardware that could be developed. Some examples,

Support for temperature regulation monitoring.

Direct connection to filter wheels.

Use of the camera as a stand-alone auto guider

Intelligent readout modes that can adjust sensitivity and resolution on a pixel-by-pixel basis.

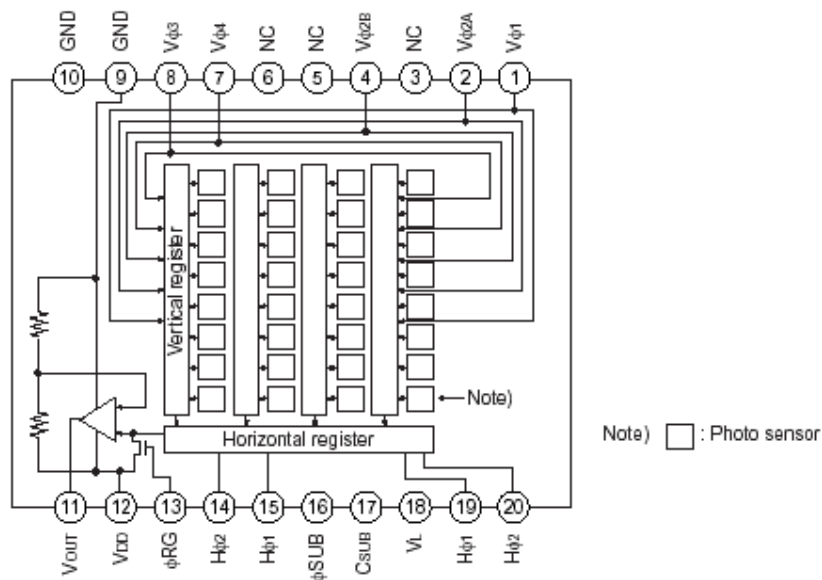
Integrated MP3 player ☺

More...

A brief introduction to astronomical CCD cameras.

This has been the subject of several lengthy books so I will try to keep this simple and refer you to the excellent primers at the end of this section.

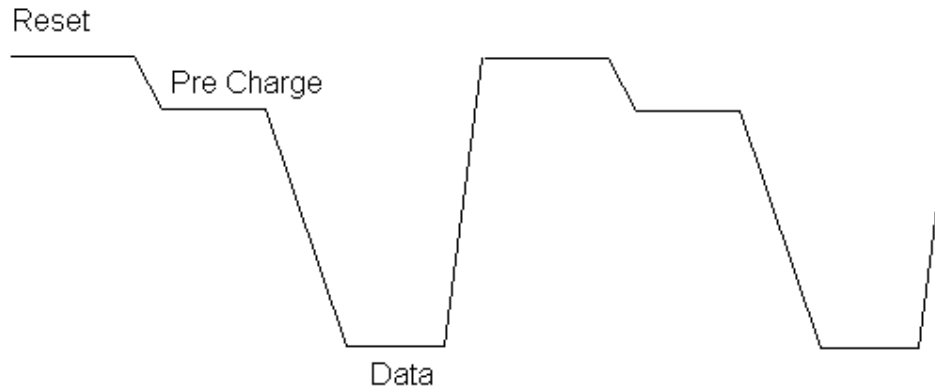
Starting with the CCD itself. This is the device that will turn the light coming from the sky into electrical signals the camera can process. The light liberates electrons that collect in the photosites (pixels) on the CCD chip. The readout process starts with a charge transfer pulse (CTP) that moves the charge collected into the CCD's vertical registers. The vertical clocks (pins 1,2,7,8 below) are responsible for moving the charge/image down the CCD one row at a time with the bottom rowing being move to the horizontal register. The horizontal register clocks can then move this charge one pixel at a time into the output stage of the CCD.



Graphic from the ICX285 datasheet

To read a pixel the output stage is first cleared of charge by clocking the reset gate (pin 13). After this has happened the output from the CCD amplifier (pin 11) is at an initial or precharge level. The horizontal registers (pin 19,20) then moves one pixel worth of charge into the output stage where it is amplified to give a data level. The difference between the precharge level and the data level is inversely proportional to the light that fell on the pixel.

Typical output from CCD



The signal from the CCD varies from about 11V for precharge and dark signals to 10V for bright, saturated signals. The usual method to process these is called correlated double sampling. The precharge and data levels are both stored on capacitors and an amplifier outputs the voltage difference between the two levels. This neatly removes the 10V offset. Also the amplifier can be set to invert the signal so increasing voltage = increasing light and also amplify the signal to meet the needs of the analogue to digital converter (ADC).

Due to the faintness of astronomical targets in general long exposures are often required in order to collect enough light. During these long integrations noise can also be added to the image being built up in the CCD. Thermal noise effects pixels unevenly with some pixels being termed 'hot' and saturate quickly while others more slowly accurate dark current. These effects are reduced by cooling the CCD. The amplifier on the CCD chip produces electroluminescence that appears as a glow coming from one corner of the CCD. Switching off the amplifier until it is needed for read out can eliminate this.

The ADC's job is to take voltage from the CCD and convert it to a numerical value. The precision it can do this to is limited by a number of factors especially the number of bits it uses to represent the numbers. Eight bit converters can represent numbers from 0-255, 12 bit 0-4095, 14 bit 0-16383 and finally 16 bit 0-65535. The number of bits needed to completely digitise a signal without loss of information is determined by the dynamic range of the CCD. A typical CCD might have a max signal corresponding to 60000 electrons (well depth) and a noise level corresponding to 10 electrons. By dividing 60000 by 10 we get the dynamic range, 6000 in this case. So a 14 bit ADC provides more than enough dynamic range in this example.

After digitisation the information needs to be move to a computer. Older cameras used the parallel port for this function, however this method is becoming obsolete with modern computer operating systems shunning real time control of hardware. High-speed serial protocols are now generally used.

There is so much more that could be discussed here but instead let turn our attention to the specifics of the Artemis.

References

For much more information on CCD cameras you could read the following from Kodak.

<http://www.kodak.com/US/en/digital/pdf/ccdPrimerPart1.pdf>

<http://www.kodak.com/US/en/digital/pdf/ccdPrimerPart2.pdf>

And the interactive online primer from Roper

<http://www.roperscientific.de/theory.html>

The Artemis CCD camera.

As a whole the Artemis camera is quite a complex device. In order to understand it better lets consider the camera one section at a time. The CCD sensor is a good place to start.

The CCD

At the moment the camera only supports CCDs from Sony's exview range. These offer the extremely good performance in astronomy for the price. Originally designed for use in low light and IR illuminated security cameras they have very good sensitivity and wide response from blue to IR. Also being intended for use in mass-produced consumer items they are designed to need the minimum of support components and are sold at a reasonable price.

The camera can be set up to run the ICX285,429,245,255 and more may follow. All these chips can be run with 4 vertical clocks, two of which are 2 voltage level (0V and VI) and two 3 voltage level (0V,VI,and Vh). In all cases Vh is 15V and VI is -7V except the ICX249 which is -9V. The horizontal and reset signals are simple 0-5V levels although the CCD does apply a DC offset to the reset gate clock. The substrate clock again has a DC bias applied and swings between VI and Vh in order to clear the CCD of any charge without need to readout the whole CCD. The CCD socket on the Artemis PCB is termed a universal socket. Its set up such that the ICX285 could be plugged straight in. However as the ICX285 has a number of pins that are not used we can put other signals in these positions. Then using small adaptor boards the ICX255, 254 and 429 can be plugged in to the same socket.

The Sony CCDs in some ways try to do a little too much. The power supply for the chip supplies the amplifier and a circuit that generates the bias on the substrate. In order to eliminate the amplifier glow during integration we need to switch off this circuit. However doing this also removes the bias on the CCD, which results in a very dramatic reduction in well depth and hence dynamic range. In order to overcome this we will inject a DC bias. This approach is specified for many of the Sony CCD's but not ICX255,254 and 285; however it works well with these.

Signal conditioning pre ADC.

The output from the CCD needs to be buffered before we can process it. A JFET transistor with high input impedance is used for this stage. For most cameras the next stage should be the correlated double sampling (CDS) circuit however the Artemis does the precharge subtraction in software. This approach is consistent with our goal of doing as much in software as possible and open up a few options to us and is worth considering in more detail. For a standard CDS stage the precharge level is amplified then gated and stored on a capacitor. Next the data level is likewise amplified and gated on to a different capacitor. After these stages are complete the difference in the charge on the two capacitors is again amplified and it is this signal that is digitised. So we see that there are a number of analogue stages that are susceptible to noise degrading the signal. It is certainly possible to achieve good digitisation this way but also several stages where problems could occur. Coming from an unconventional imaging background I wanted try something different. Andrey Filippov had written an interesting article on "An Alternative to the Correlated Double Sampling (CDS) and Binning in CCD Readout" available on line at <http://www.elphel.com/articles/CDS.html> His suggestion is to digitise precharge and data directly without subtracting the two levels in hardware. Then the precharge level is subtracted from the data level in software that is somewhat easier and less susceptible to noise. The current version of the cameras firmware can either send both precharge and data levels to the PC or it can subtract the precharge itself then send just the 16bit result.

This is only touching the surface of the possibilities though. A low quality high-speed focus mode may be possible where the precharge level is not used. More intriguing is the potential for variable binning.

During readout the charge from a pixel is moved into the output stage of the CCD. This is a non-destructive process; the only thing that will delete this information is the reset gate. Then we can assess the pixel level, if its low we can clock another pixel into the output stage and measure again with the output now being the sum of 2 pixels. Other options could be investigated such as multiple sampling or precharge etc. The downsides of this method include the fact that we get 2 lots of digitisation noise and that double the amount of information need to be dealt with in software. Advances in ADC design and speed of microcontrollers may mean that this is an approach whose time has come!

Back to the camera the CCD output which varies between about 10 and 11V is fed to the op am circuit. In one go this subtracts an 11V offset, amplifies the voltage about 5 times, then inverts the signal and take into account any drift in voltage levels with temperature. The circuit is adjusted to give dark and precharge values of about 1V while 5V corresponds to a saturated pixel.

Analogue to digital conversion.

This uses the TI ADS8322 16 bit ADC. Its range is set to 0-5V, however as the precharge level is 1V the data from the CCD falls in the range 1-5V. At first sight this might appear to limit the dynamic range of the CCD. Remember that these CCD are only really producing 13-14 bits of data so digitising in 4/5 of the full range of the 16 bit ADC is not doing to limit at all. The 8 bit parallel output from the ADC goes direct to the cameras databus which is shared with the microcontroller, FIFO memory and the USB module. So data can go to the microcontroller to be stored and analysed before being passed to the PC OR the data can go straight from the ADC to the USB port for speed.

The Processor.

This is a very nice reprogrammable device from microchip. These are supplied by use with a non erasable boot code in low memory and with the upper memory blocks free. This gives the pic some very limited functionality importantly including the ability to reprogram these upper memory blocks from data it receives from the USB port. When the camera receives a command it first checks if corresponds to those in the boot section. If not the value of the command is passed to the upper memory where any code that is present can act on it.

Peripherals

The camera is provided with a standard guide socket to plug into a compatible mount such as an LX200. These work by sensing the levels on four inputs that the scope pulls high. There is one input per NSEW direction. If the camera pulls the line low the scope will move in the corresponding direction and the set guide speed. In order to provide protection to the mount and camera the communication occurs through optical isolators.

It is envisaged that this camera will often be used in conjunction with a guide camera. To give some flexibility a single output is reserved to controlling the exposure from a modified webcam. The webcam would still need to be plugged into the USB port of the computer but exposures can be controlled by the cameras port rather than needing the parallel port of the PC and another lead to the telescope.

Expansion port.

The camera features an expansion port. This is a 4 wire connector providing 5V and Gnd for power and a 2 wire serial interface. The firmware contains a protocol for talking to multiple devices in this port. The protocol is a master (the camera) slaves (anything else) arrangement. Through this link we can add extra functionality eg filter wheel control, or even adaptive optics/micro guiding if we can develop the hardware needed.

USB chipset.

The USB chipset from is from FTDI. It is limited to USB1.1 speeds but provide so much functionality that makes it attractive. It has 2 onboard FIFO buffers so to the microprocessor USB communication is a simple as reading and writing to a memory chip. This storage means the processor need not stop what its doing when a command comes in and neither does it have to wait until the PC is listening before sending data. The exception is if the buffer fills up. The PCB has an eeprom we can program with the cameras name and numbers that specify a unique set of plug and play drivers to be install to support it.

FIFO memory.

On slower computers, or congested USB networks the readout procedure can stall for a few milli seconds from time to time while the computer does something else. Any pixels left in the horizontal register in this time are subjected to increased levels of dark current especially those closest to the output stage of the CCD. To avoid this situation the camera supports an optional FIFO memory buffer. This can hold all the data generated from a single line of the CCD so when ever a stall occurs the horizontal buffer can still be read to completion.

Credits.

QCUIAG

First and foremost we would like to thank the members of [QCUIAG](#) for their support over the years that have led from modifying webcams and security cameras to the Artemis camera.



Mechanical Design

To [Arthur Edwards](#) who has designed and machined the case for the Artemis camera as well as the many prototypes.

PCB Layout

To [John Moore](#) for laying out the printed circuit boards and patients working with a design that must have appeared to be constantly changing.

Beta testers

A huge THANK YOU to our intrepid group of beta testers for their testing, suggestions and encouragement.

[Tomi Virtanen](#)

[Martin Burri](#)

Martin Farmer

Stuart Hutchins

[Steve Hill](#)

Neil McMurtrie

[Peter Vasey](#)

[John Moore](#)

Thank you all.

[Steve Chambers](#)

[Jon Grove](#)